An Update on the Timepix2

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The Principal Acknowledgments

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Medipix2 Design Team

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And

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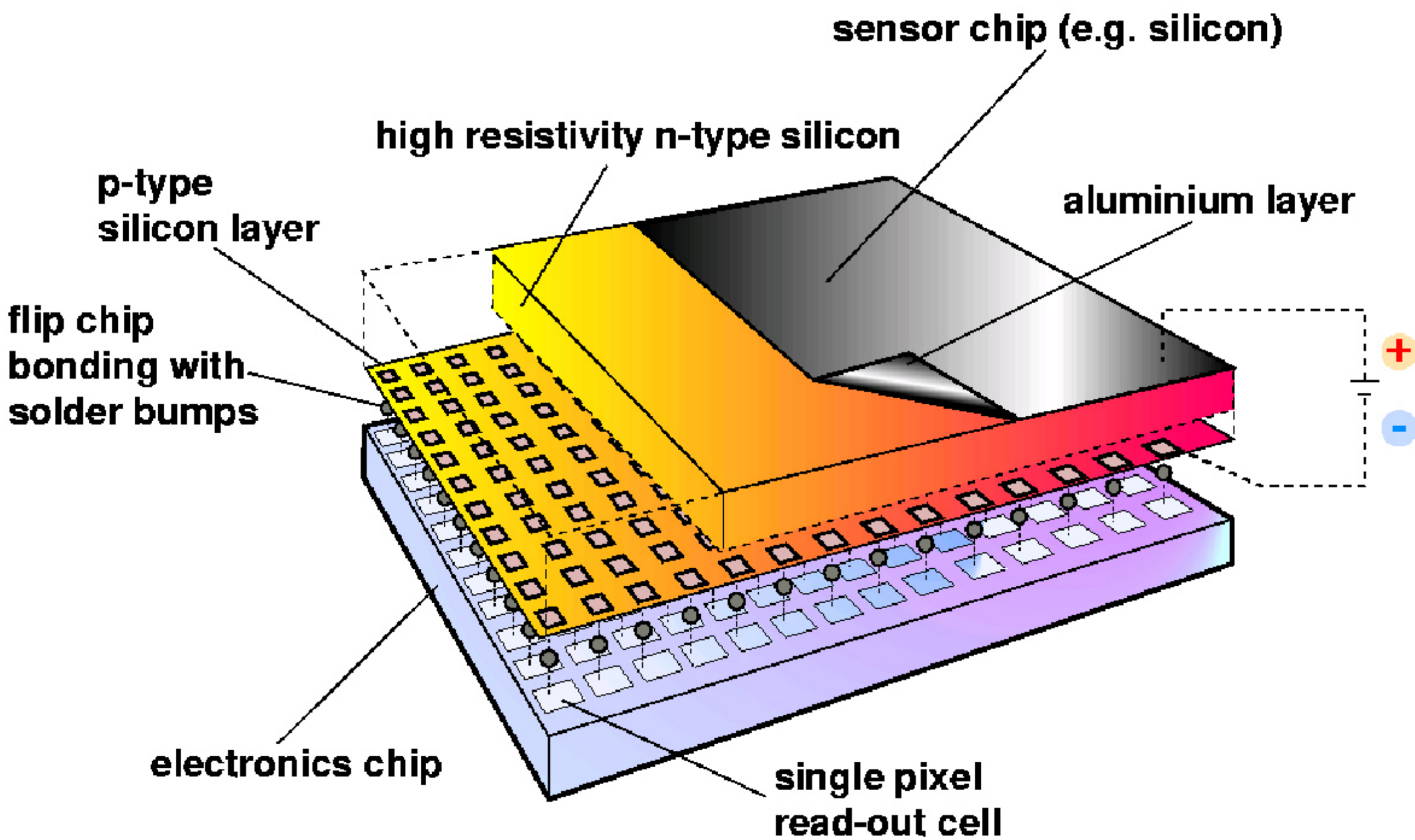
Some Medipix Collaborations Genealogy

- **Medipix (1)—Formed in the early 1990's and ended with the formation of Medipix2…**
  - **Medipix Chip—64 x 64 170μm pixel Photon Counting (PC)**
- **Medipix2—Formed in the late 1990's (still active)**
  - **Medipix2 MXR—256 x256 55μm 2-Threshold PC Frame (250μm IBM)**
  - **Timepix (2006)—256 x256 55μm TOT *or* TOA & PC Frame (250μm IBM)**
  - **Timepix2 (2018)—256 x256 55μm TOT+TOA & PC Frame (135μm TSMC)**
- **Medipix3—Formed in 2006 (still active)**
  - **Medipix3, Medipix3.1…**
  - **Medipix3RX (~2012)—256 x256 55μm pixel, Charge Summing PC**
  - **Timepix3 (2014)—256 x256 55μm pixel TOT+TOA & PC Frame & Data-Driven Readout… (135μm IBM)**
- **Medipix4—Formed in late 2016 (just starting up)**
  - **Medipix4 (PC) and Timepix4 (TOT+TOA & PC) Frame & Data Driven (65μm TSMC) Pixel size and number TBD…**

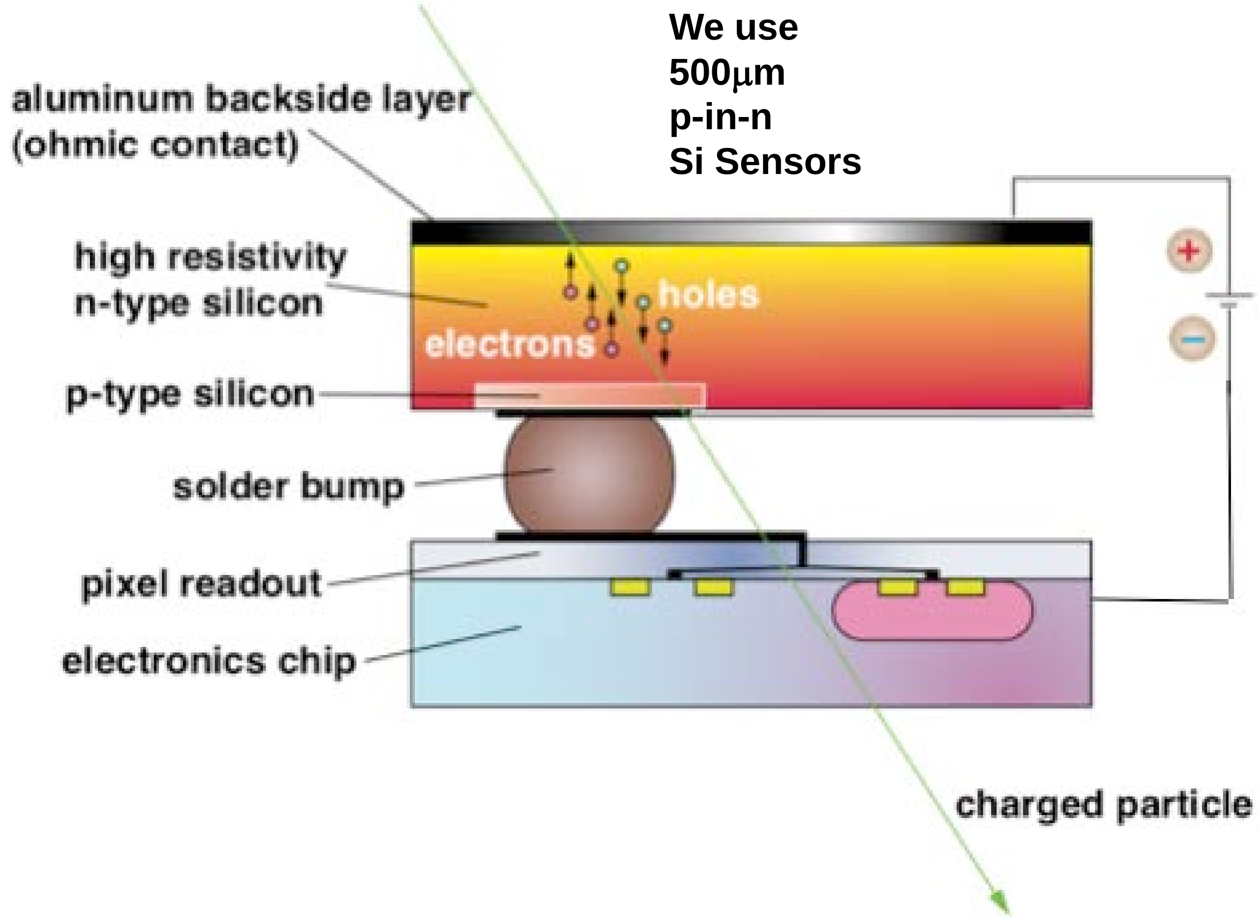
Hybrid Pixel Detectors



Detector and electronics readout are optimized separately
Bonding is done with the FlipChip ® process…

Schematic Cross Section of a Hybrid Pixel Detector for Penetrating Charged Particles

We use
500μm
p-in-n
Si Sensors

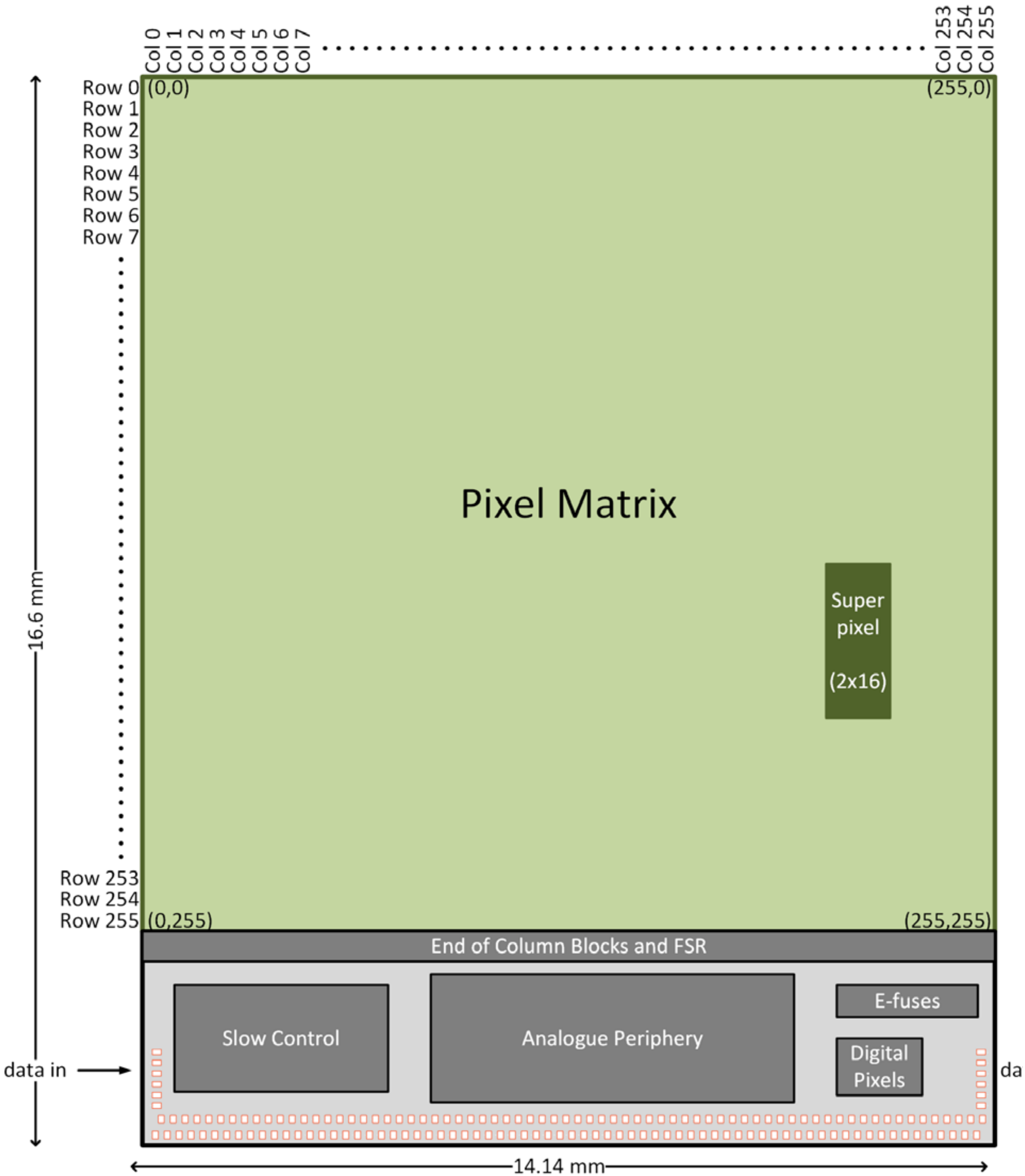


Digitization Methods

- **Time-Over-Threshold (TOT)**
  - **This is a “Wilkison” type Analog to Digital Convertor (ADC)**
  - **A “Pulse-Shaping” circuit regularizes the input current into a pulse whose pulse-height is proportional to the total charge collected over the shaping time.**
  - **The input voltage pulse is matched to a Threshold discriminator to output a digital “1” level for the duration of the time that the input is above the Threshold.**
  - **The input voltage is discharged by a constant current during which a clock is counted to determine the digital value for the input charge.**
- **Time-Of-Arrival (TOA)**
  - **The discriminator output described in the TOT method above, triggers a counter to begin counting as soon as the digital level changes to “1”.**
  - **The end of the Frame stops the TOA counters. (A Common Stop Time to Digital Convertor (TDC).**
- **The clock frequency limits the resolution in both cases…**

UPDATE ON Timepix2

On behalf of the Medipix Design Team of CERN



130 nm CMOS
28 bits/pixel
Simultaneous ToT and ToA
Separate ToT and ToA clock freq.
Readout dead-time-free modes
Fast clear

Digital and analogue test pulses
Digital and analogue pixel masking

- **ROI**
- **coarse pitch bump bonding**

Adaptive frontend gain
Reduced threshold dispersion

Digital diagnostics modes
Test points in analogue frontend

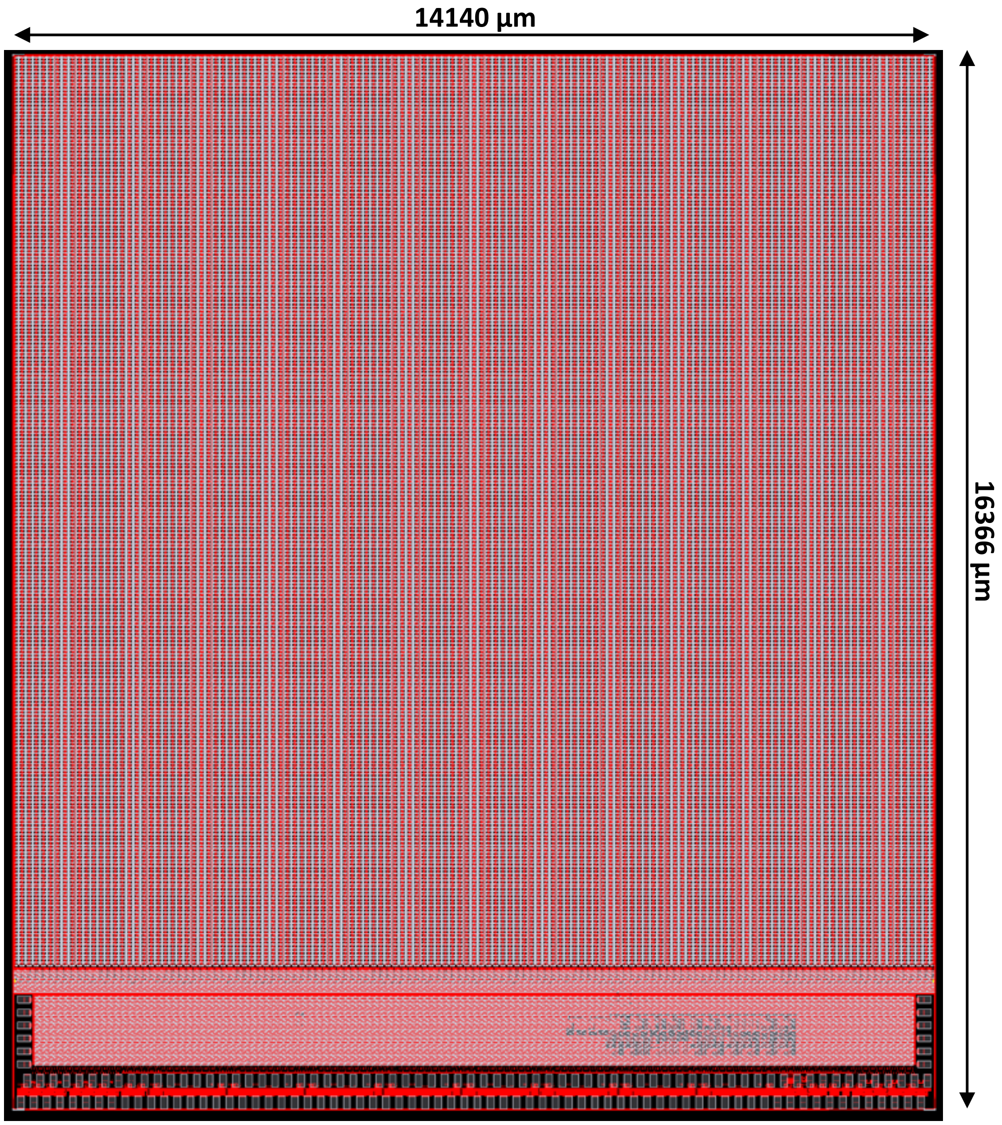
Matrix occupancy monitor
Digital-only pixels with wirebond input

Serial port (full frame)
32b Parallel port (full frame)
Serial port (zero column suppression)

Serial port daisy-chaining
IO compatible with TSVs

Timepix2

	Timepix	Timepix2
Size [µm]	14111 x 16120	14140 x 16366
Pixel size	55 x 55 µm^2	55 x 55 µm^2
Pixel pads size	20 x 20 (octagon)	12 x 12 (octagon)
Pads pitch [µm]	120	200 (100 staggered)
Number IO Pads	127	150
TSV ready	NO	YES
Differential pads	LVDS	SLVS



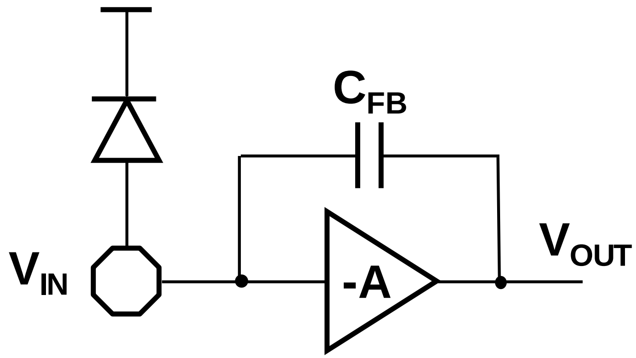
X. Llopart

Parameter	Value
Technology	TSMC 130nm CMOS
Number of pixels	256 x 256 @ 55 um pitch
Analog front-end size	~55 x 14 um
Analog supply voltage	1.2 V
Detector capacitance	50 fF
Front-end gain	Linear, possibility to configure for “logarithmic” gain mode only in positive polarity
Detector polarity	Both Electron collection: • Leakage current compensation optimal ($I_{DET}>I_{KRUM}$) • Non-monotonicity of the ToT vs Qin Hole collection • Leakage current limited ($I_{DET}<I_{KRUM}/2$) • Logarithmic gain mode available
Leakage current	Electron collection: Up to 12nA/pixel Hole collection: 2nA/pixel
Minimum threshold	$\boxed{\text{~600e-}}$ 2.16 KeV
Peaking time	~100 ns (Adaptive gain=0) ~200ns (Adaptive gain=1)
Operating temperature	-20ºC<T<70ºC
Power consumption	5uA/pixel @1.2V i.e. ~165mW/cm^2 (low power mode)
Analog Power masking	Available per pixel (2.6 ms to load configuration bits)

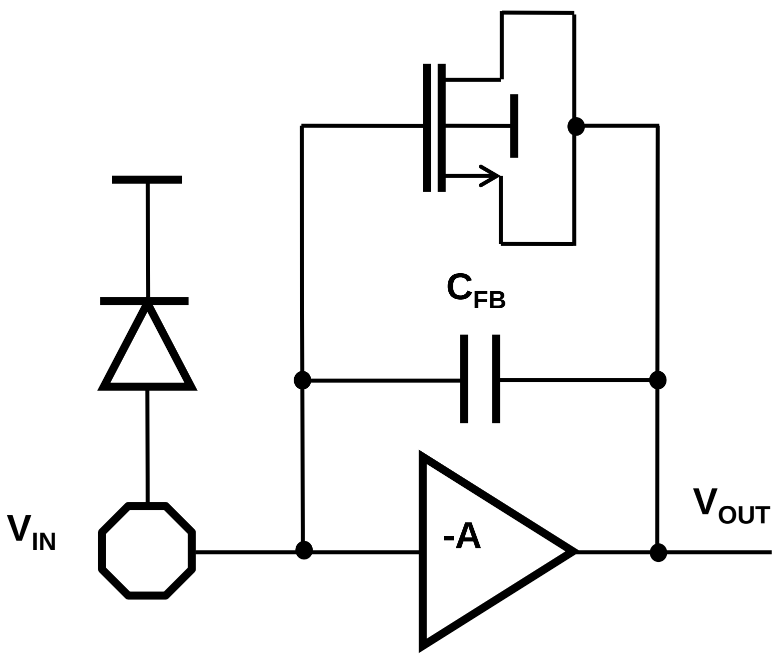
- Adaptive gain OFF
  - Gain ~25mV/ke-, Noise ~60e- r.m.s., Threshold dispersion ~30e- r.m.s. Minimum threshold ~400e-, Peaking time ~100ns
- Adaptive gain ON
  - Gain ~20mV/ke-, Noise ~55e- r.m.s., Threshold dispersion ~40e- r.m.s. Minimum threshold ~400e-, Peaking time ~200ns
- Monotonic ToT amplitude up to 3.42MeV (Si)

R. Ballabriga

Voltage-dependent feedback capacitance

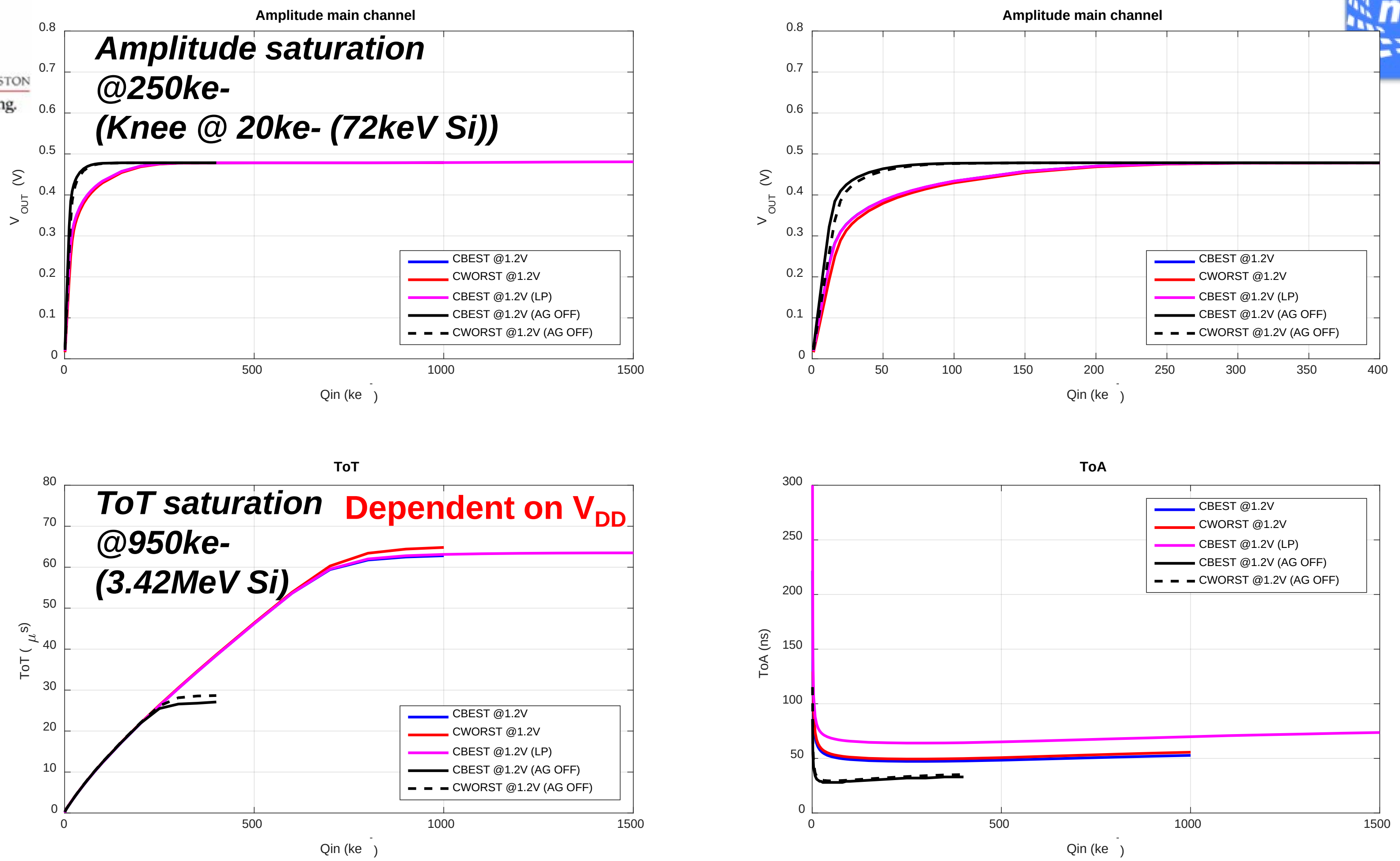


$$\frac{\Delta V_{OUT}}{\Delta Q_{IN}} = \frac{1}{C_{FB}}$$



When the transistor is active, the feedback capacitance is ~125fF
(Dimensions transistor 1/10)

M. Manghisoni et al. "Dynamic Compression of the Signal in a Charge Sensitive Amplifier: from Concept to Design" IEEE Trans. Nucl. Sci. Vol. 62, No. 5, 2015



Amplitude, ToT and ToA for the front end with adaptive gain ON, front end power supply 1.2V

(a low power mode for the discriminator is also considered and has an impact on the ToA (discriminator propagation delay))

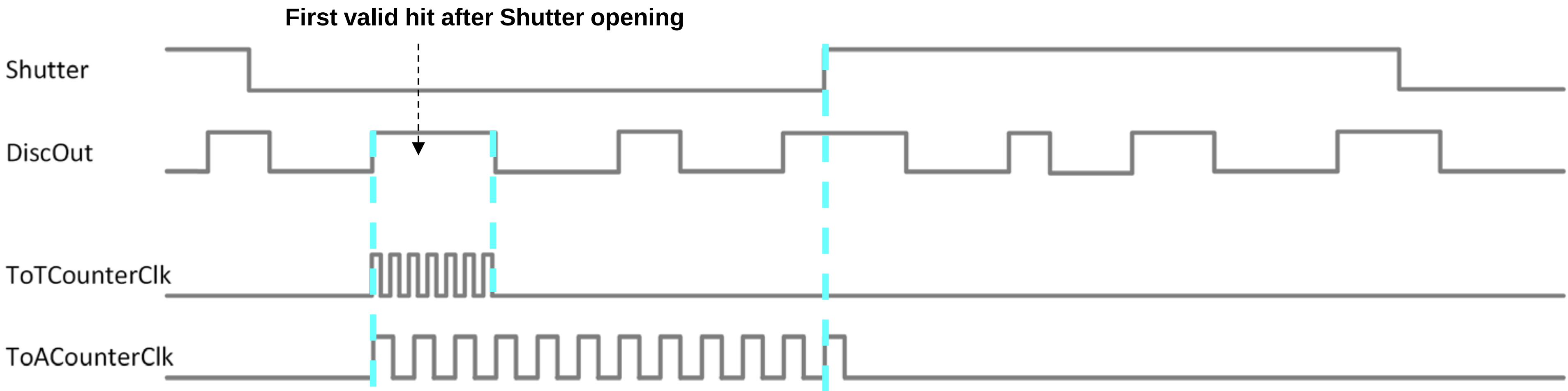
(Gain: ~20mV/ke- (CBEST), ~16mV/ke- (CWORST))

Pixel Digital Operating Modes

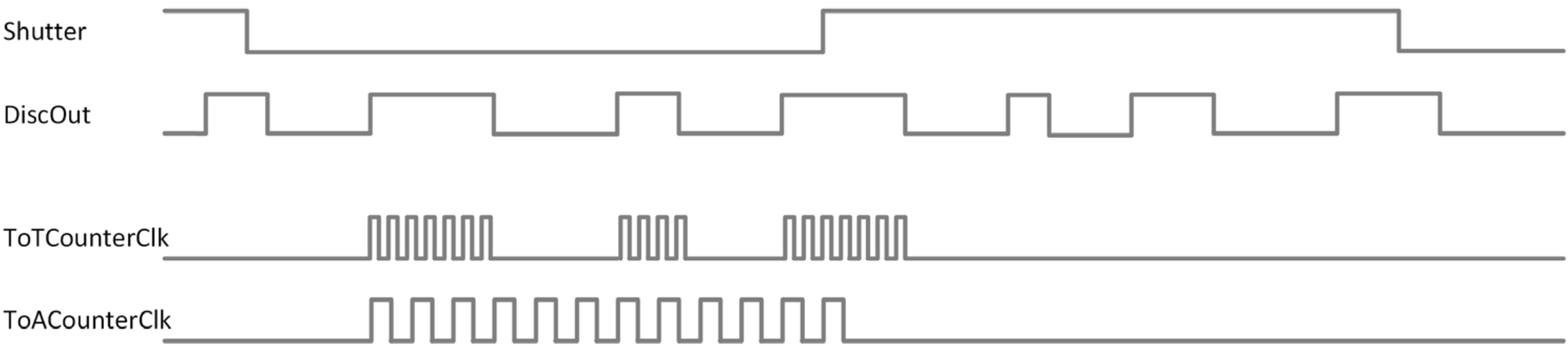
28 bits/pixel:
2 x 4b chains
2 x 10b chains

Mode Name	Description	1^{st} Counter	2^{nd} Counter
ToT10/ToA18	Simultaneous ToT and 1^{st} hit ToA* Mode options (programmable): 1) 1^{st} hit or integral ToT 2) Overflow (wraparound) of ToA counter	10-bit ToT	18-bit ToA
ToT14/ToA14		14-bit ToT	14-bit ToA
ContToT10/Event4	Continuous read/write ToT Mode options: 1) 1^{st} hit or integral ToT (programmable) 2) Supplementary 4-bit eventing counting (readout optional)	10-bit ToT 4-bit #Events	10-bit ToT 4-bit #Events
ContToT14	Continuous read/write ToT Mode option: 1^{st} hit or integral ToT (programmable)	14-bit ToT	14-bit ToT
ContToA10	Continuous read/write 1^{st} hit ToA	10-bit ToA	10-bit ToA
ContToA14		14-bit ToA	14-bit ToA
ContEvent10	Continuous read/write event counting	10-bit #Events	10-bit #Events
ContEvent14		14-bit #Events	14-bit #Events

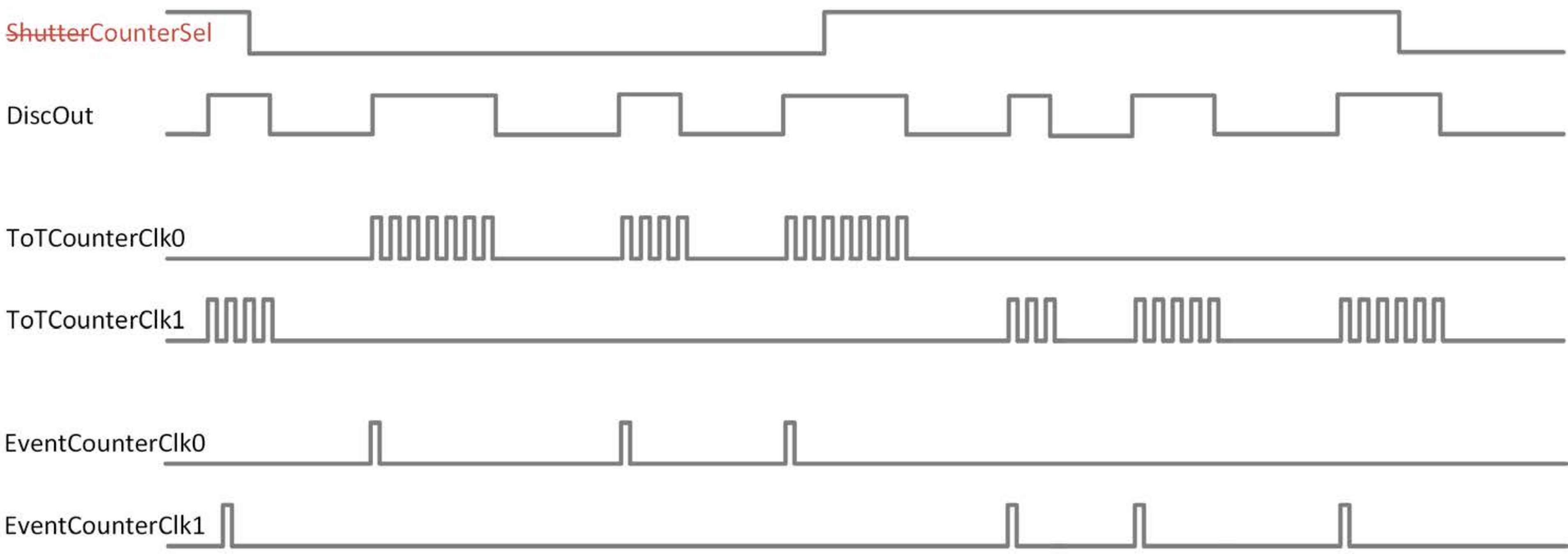
Mode Name	Description	1st Counter	2nd Counter
ToT10/ToA18	Simultaneous ToT and 1st hit ToA*	10-bit ToT	18-bit ToA
ToT14/ToA14	Mode options (programmable): 1) 1st hit or integral ToT 2) Overflow (wraparound) of ToA counter	14-bit ToT	14-bit ToA



Mode Name	Description	1st Counter	2nd Counter
ToT10/ToA18	Simultaneous ToT and 1st hit ToA*	10-bit ToT	18-bit ToA
ToT14/ToA14	Mode options (programmable): 1) 1st hit or integral ToT 2) Overflow (wraparound) of ToA counter	14-bit ToT	14-bit ToA



Mode Name	Description	1st Counter	2nd Counter
ContToT10/Event4	Continuous read/write ToT Mode options: 1) 1st hit or integral ToT (programmable) 2) Supplementary 4-bit eventing counting (readout optional)	10-bit ToT 4-bit #Events	10-bit ToT 4-bit #Events
ContToT14	Continuous read/write ToT Mode option: 1st hit or integral ToT (programmable)	14-bit ToT	14-bit ToT



Power Consumption in the Matrix

- **Analogue:**
  - **5 µA/pixel @ 1.2 V**
  - **Unused pixels can be powered down to a few nA**
  - **With all 65536 pixels powered up: <400 mW**

- **Digital:**
  - **0.24 mW/superpixel during open Shutter in simultaneous ToT/ToA mode with 100 MHz ToTClk and 100 MHz ToAClk, assuming sparse activity and superpixel clock gating enabled**
  - **ToT and ToA clocks can run at lower frequencies**
    - **ToAClk is output from a clock divider taking ToTClk as input**
  - **The clocks in a double column are disabled when all pixels in the double column are masked**
  - **Full matrix digital power with sparse activity and 100 MHz clocks: <500 mW**

- **Total: <900 mW for the full matrix assuming sparse hits and both clocks @ 100 MHz**
  - **~2 W for the full matrix in cases of full occupancy (not relevant to dosimetry)**

Maximum Frame Rates

With a 100 MHz DCLOCK_IN:

# bits	Full frame, serial port		Full frame, parallel port		Zero column suppression, serial port	
	Time to Read [ms]	Max framerate [fps]	Time to Read [ms]	Max framerate [fps]	Time to Read [ms]	Max framerate* [fps]
10	6.55	153	0.2	4883	0.41	2441
14	9.18	109	0.29	3488	0.57	1744
28	18.4	54	0.57	1744	1.15	872

*The framerate in ZCS mode depends on the matrix occupancy. The rate reported here is the theoretical maximum, which assumes only 16 columns of data are output from the chip.

Timepix2 v. TImepix

1. Improved Front-End TOT range and stability…
2. Simultaneous TOT an TOA (10 ns)…
3. Stable performance with 100 MHz clock…
4. Stable and linear internal digital and analog test pulses…
5. TSV capable (no wirebonds & secure mounting)…
6. 28-bit (Fungible) output buffer…
7. Improved DAC stability…
8. Multiple continuous operational modes…
9. Can use Timepix sensors…
10. Bonus—8 Digital Pixels to couple external devices

Status

- Six wafers (~106 chips) are at CERN now, and they are undergoing probe testing to verify performance against the design simulations…

- If no issues are found, they will be sent to have Si Sensors bump-bonded later this month.

- Interfaces are being prepared at ADVACAM and IEAP.

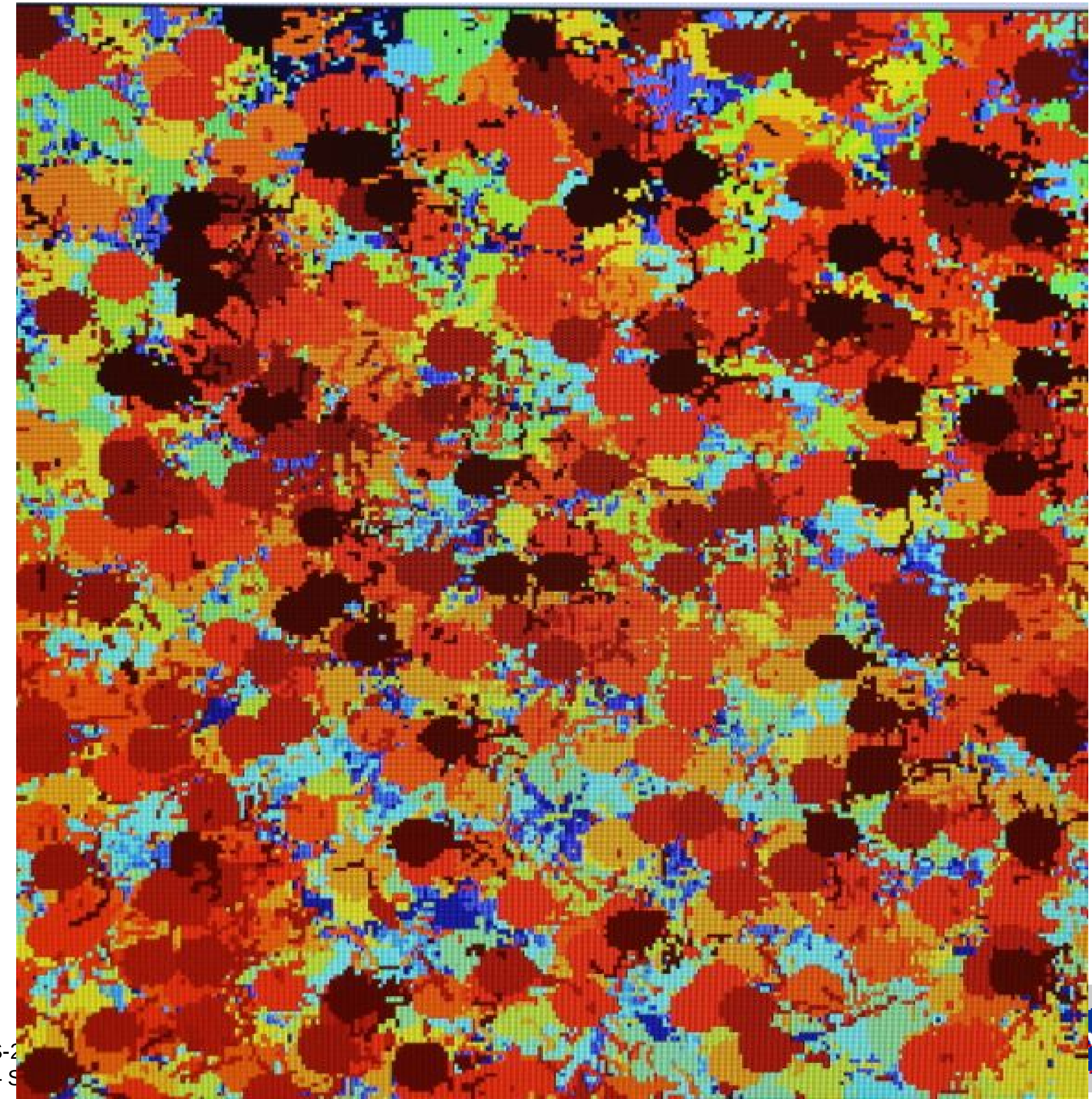
- …Expect functional devices by mid to late Nov,(2018)…

Timepix2 and Beyond

- Eventually, the Timepix2 chips should be able to replace the Timepix chips…
- It is also may be possible to modify the HERA units to accept the Timepix2,
- Eventual “Deep Space” monitors may take advantage of the Timepix2 or even Timepix4 chips…
- Current efforts are also focusing on developing Timepix2 or Timepix3-based dedicated neutron monitors…

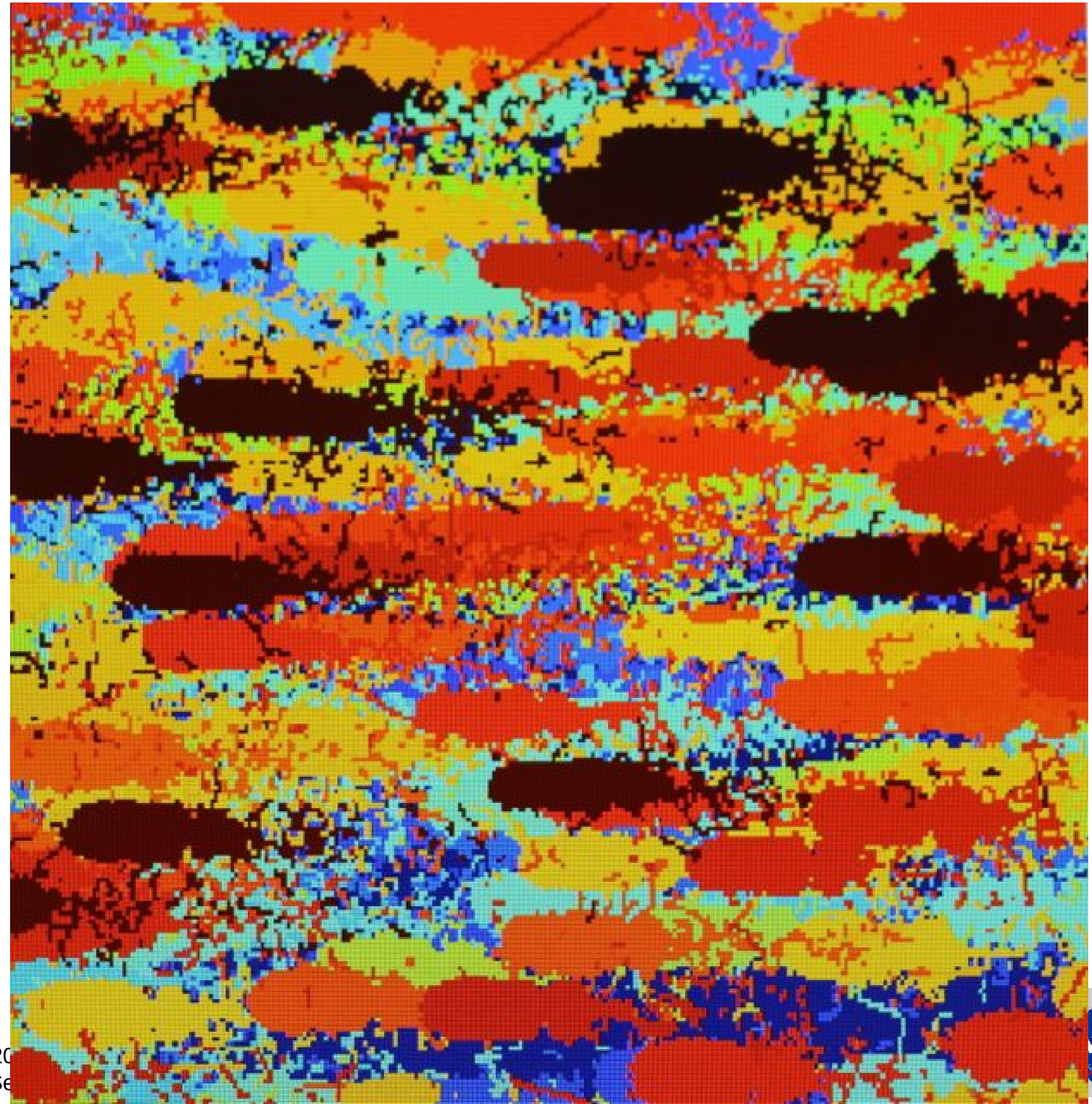

Questions…?

Timepix3 TOArt



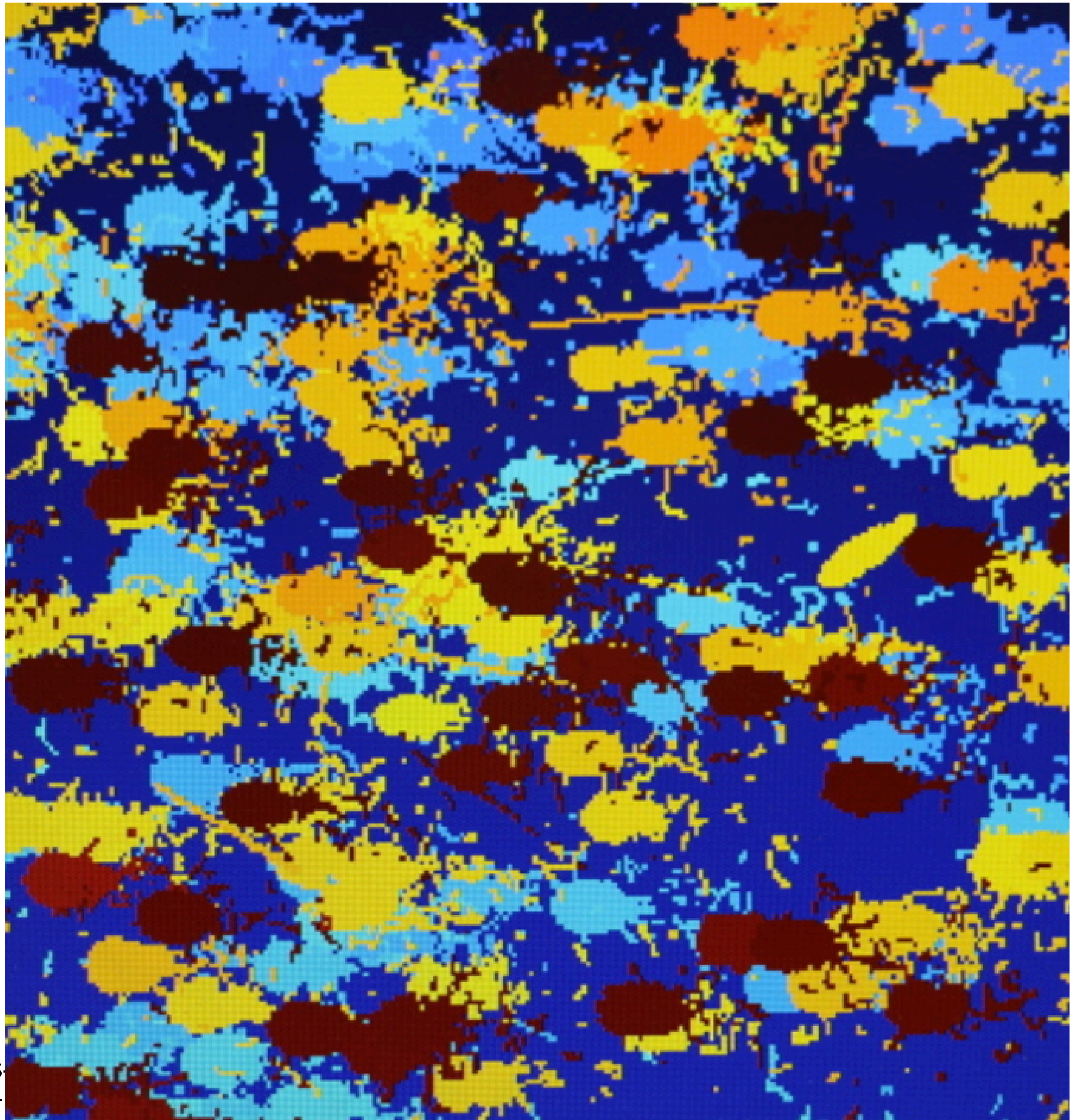
HIMAC
Fe Beam
@ 45˚

Timepix3 TOArt



HIMAC
Fe Beam
@ 75°

Timepix3 TOArt



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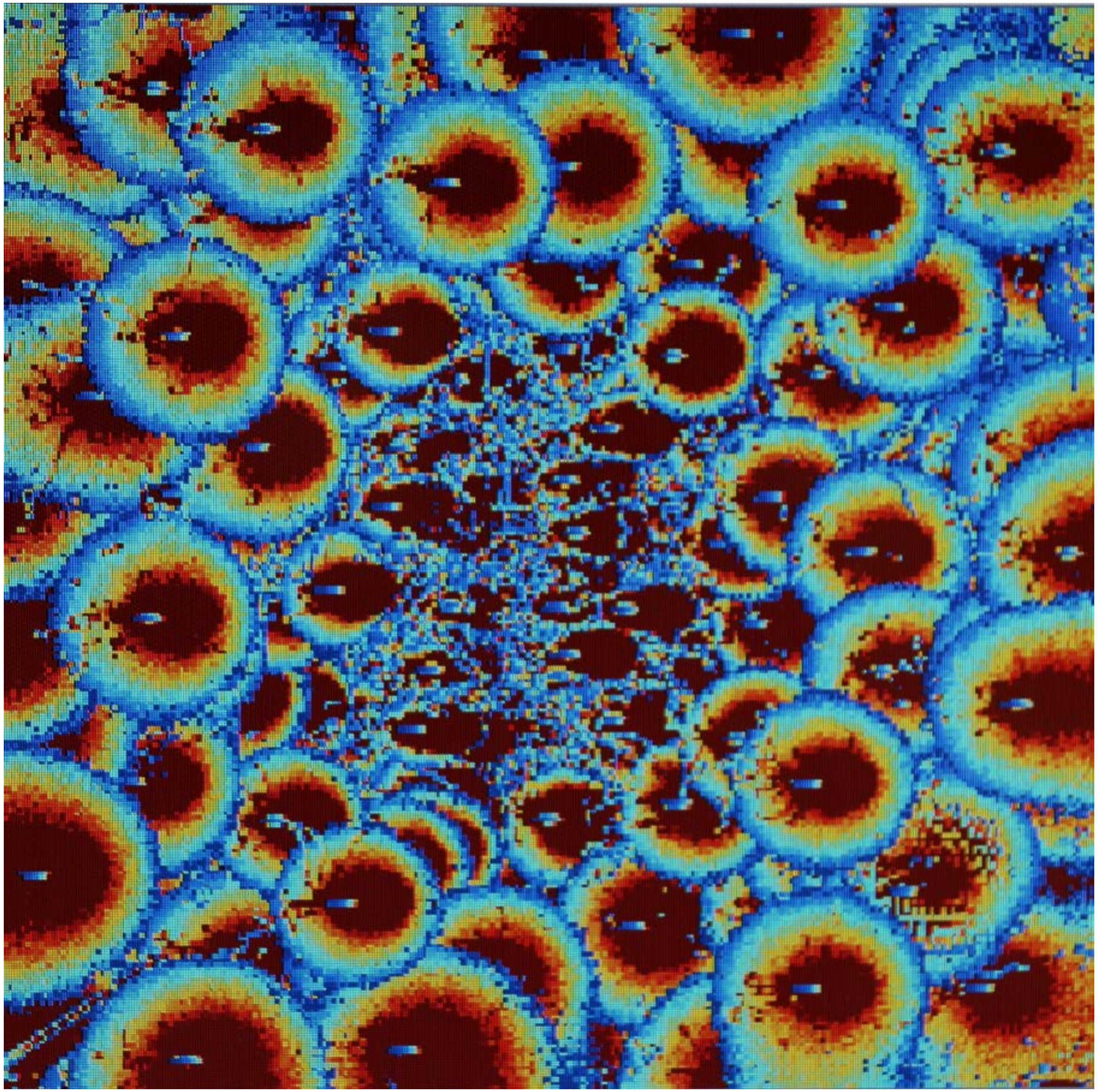
Extract From a Picture On Display at the Apple Store in Geneva

Academic non-profit Fair Use

TOTart ???

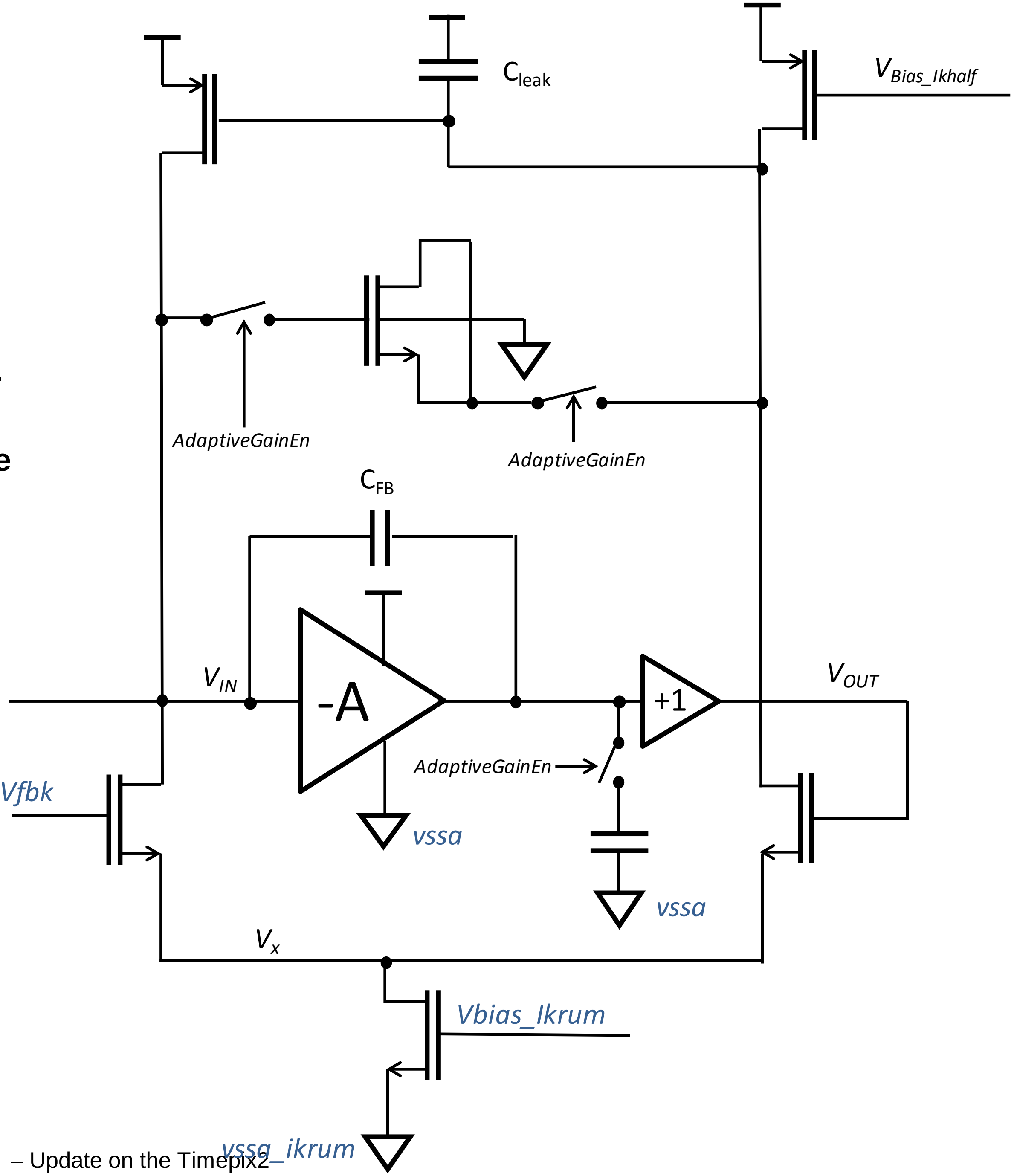


Timepix3
P-in-N
500 μm Si Sensor
w/ Low Bias V
In an Fe Beam
@ HIMAC

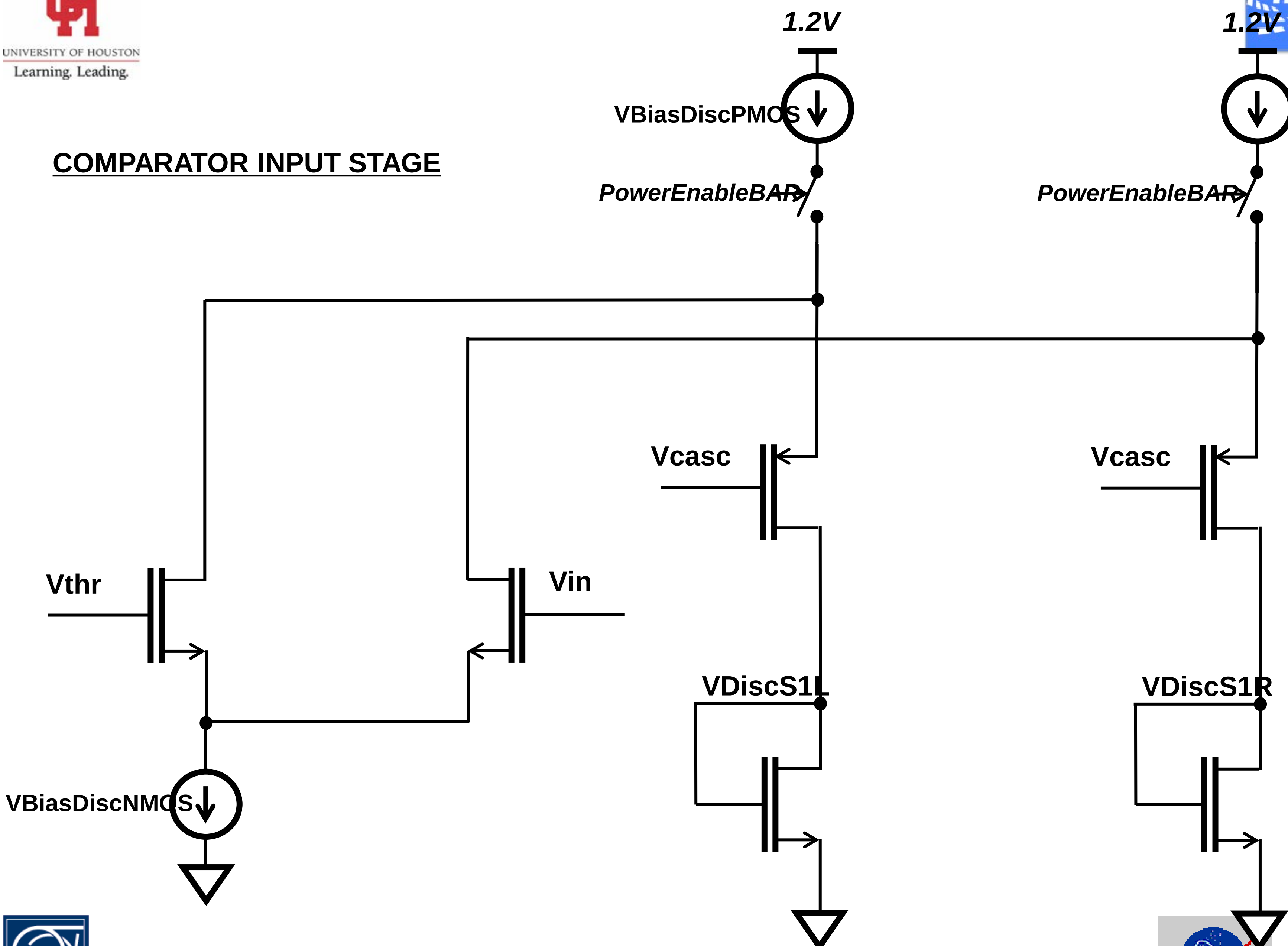
Schematics
(For the EE's in the audience)

PREAMPLIFIER

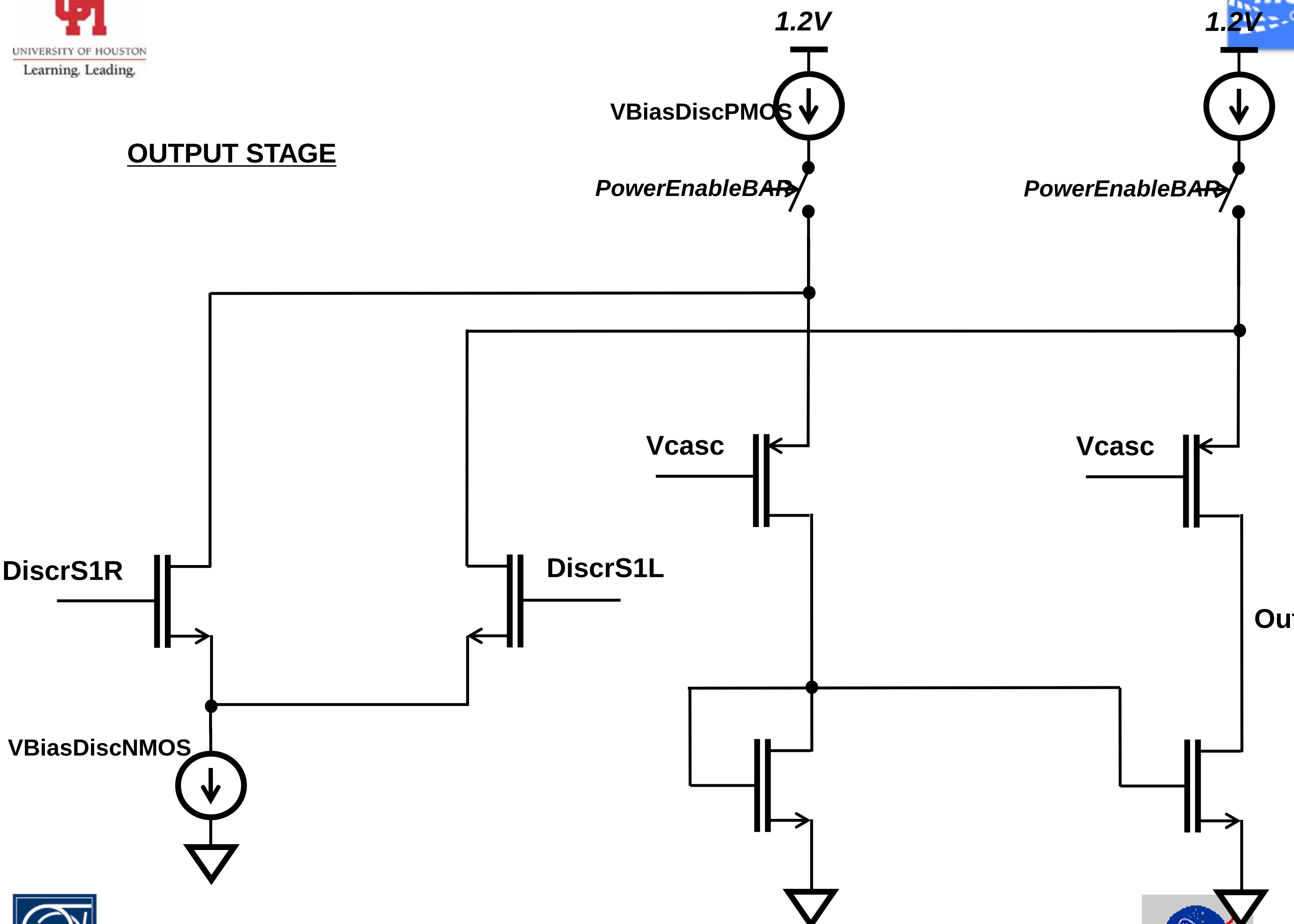
Differential amplifier
Unity gain buffer
Adaptive gain can be disabled



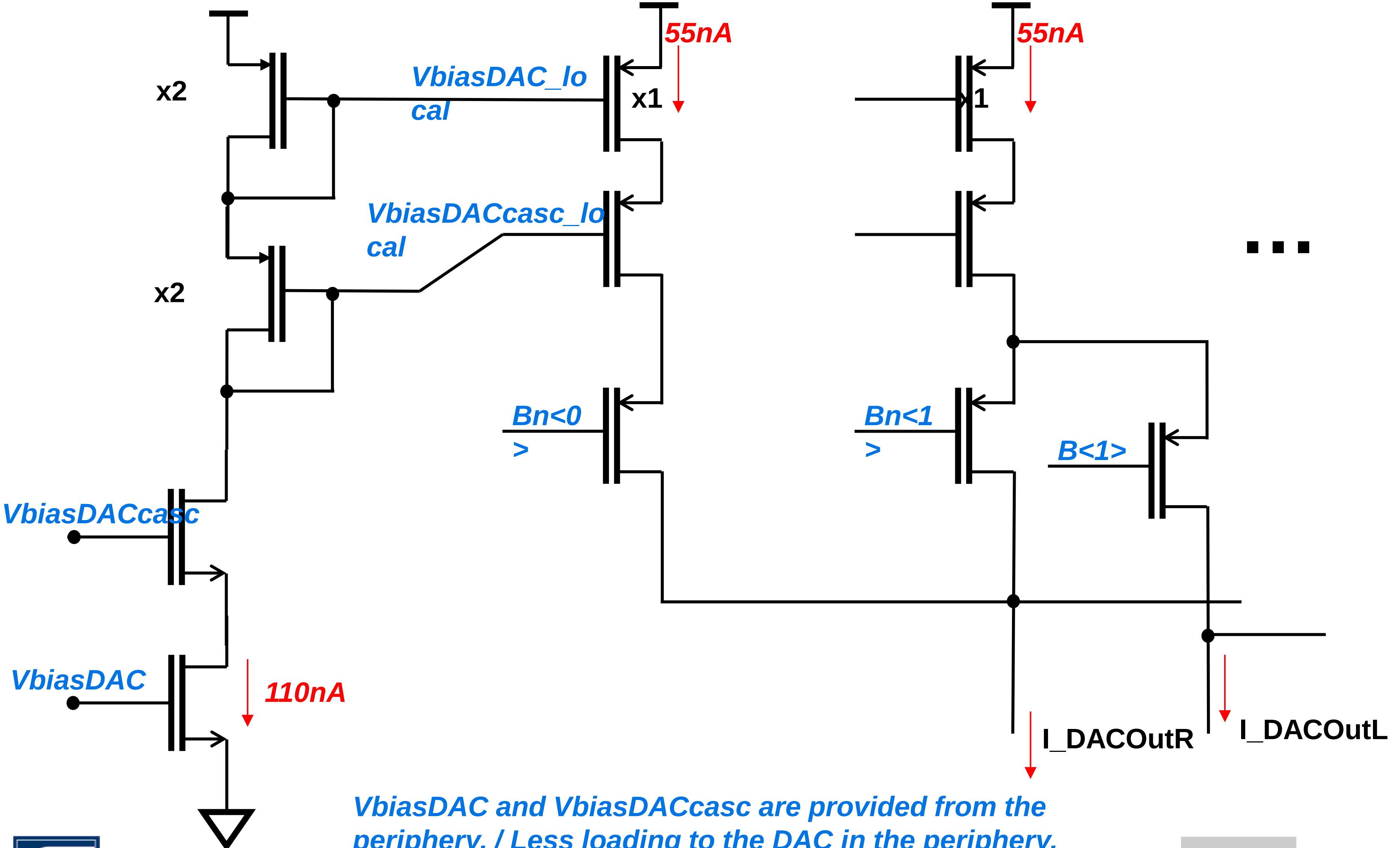
COMPARATOR INPUT STAGE



OUTPUT STAGE



Implementation of the DAC



VbiasDAC and VbiasDACcasc are provided from the periphery. / Less loading to the DAC in the periphery.